Solid-State Electronics, 1976, Vol. 19, pp. 721–729. Pergamon Press. Printed in Great Britain

AN AMORPHOUS SILICON THIN FILM TRANSISTOR: THEORY AND EXPERIMENT†

GEROLD W. NEUDECK
School of Electrical Engineering, Purdue University, West Lafayette, IN 47907, U.S.A.

and

ARUN K. MALHOTRA
Department of Electrical Engineering, Bucknell University, Lewisburg, PA 17837, U.S.A.

(*Received* 28 *October* 1975; *in revised form* 26 *January* 1976)

Abstract—The volt-ampere characteristics for a thin film transistor fabricated with vacuum deposited amorphous silicon as the semiconductor is presented. The substrate is single crystalline silicon with a 3000 Å layer of thermally grown silicon dioxide as the insulator. The gate is a buried N^+ phosphorus diffused region while the source and drain contacts are interdigited fingers of aluminum. By using the Cohen–Fritzsche–Ovshinsky model for the density of localized states in the mobility gap, the V_G vs I_D characteristic at small values of V_D is predicted and experimentally verified. This characteristic is used to theoretically predict the family of I_D curves for the TFT over a range of V_G and V_D. The theory and experiment agree exceptionally well below the gate-drain pinch-off, thereby verifying the theory of a TFT with a uniform distribution of traps in the band-gap.

NOTATION

a	slope of semi-log $g(W)$ plot
b	arbitrary constant
B	constant dependent on device parameters, (wb/la)
d	thickness of the silicon dioxide
ϵ	dielectric constant for amorphous silicon
ϵ_{ox}	dielectric constant for silicon dioxide
$g(W)$	sheet conductance of channel
I_D	drain to source current of TFT
$\rho(x)$	charge density
$\xi(x)$	band bending parameter, eV
μ_n, μ_p	mobility of electrons and holes in the extended states
l	channel length
n, p	carrier concentration for electrons and holes No./cm^3
n_b, p_b	carrier concentration into the film where no band bending occurs
η	$q\epsilon_{ox}/(dLekT)$
N_T	number of localized states per cm^3 per eV
t	thickness of the amorphous silicon film
V_D	drain to source voltage
V_G	gate to source voltage
w	width of channel
W	the potential between the gate and any point in channel

INTRODUCTION

The thin film transistor (TFT) has been under almost continuous investigation and development since the early 1960's, although its first patent application was filed in 1925[1]. Weimer[2] produced the first practical device and since then considerable effort has been put forward to improve and optimize its performance. It is still desirable to produce an all-thin-film integrated circuit on a highly insulating substrate, thereby reducing parasitic losses and spurious coupling between elements.

Several of the early TFT's used CdS as the semiconductor due to an extensive knowledge of its properties and fabrication processes developed in the research on photoconductors. Other materials used were CdSe, Te, ZnO, and SnO_2. Most semiconductors, either compound or elemental should produce devices provided that the surface and bulk states are not too large. However, the requirements for a stable and ionic motion free insulator compatible with the semiconductor eliminate a number of the possibilities.

In recent investigations van Calster and Pauwels[3] have considered the theoretical influence of surface states and bulk traps on the TFT drain characteristics, while DeMassa and Refioglu[4] have considered the case of exponentially distributed trapping centers in the semiconductor. In each case the effects on the drain current characteristics were calculated from a given model for the trap distribution or mobility function.

The purpose of this paper is to present the fabrication results and the theoretical analysis of a TFT using amorphous silicon as the semiconductor and thermally grown silicon dioxide as the insulator. Since the electrical conduction and bulk state properties of amorphous silicon have been recently explained[5, 6], a good theoretical model for the drain characteristics can be derived. We, therefore, demonstrate the possibility of a TFT with a uniform distribution of bulk states in the band gap of the semiconductor, in particular the case where the semiconductor is amorphous.

DEVICE FABRICATION

Figure 1 illustrates the cross section and top view of a completed amorphous silicon TFT. The substrate is a 1-inch wafer of ⟨100⟩-oriented single crystalline silicon of N-type doping to a resistivity of 5–25 Ω cm. Throughout fabrication, appropriate procedures were exercised so as to reduce sodium ion contamination[7]. This is necessary to prevent ionic motion in the insulator and hence hysteresis and other instabilities in the $v - i$ characteristics.

†This work was supported in part by NSF-MRL Grant No. GH33574-A3.

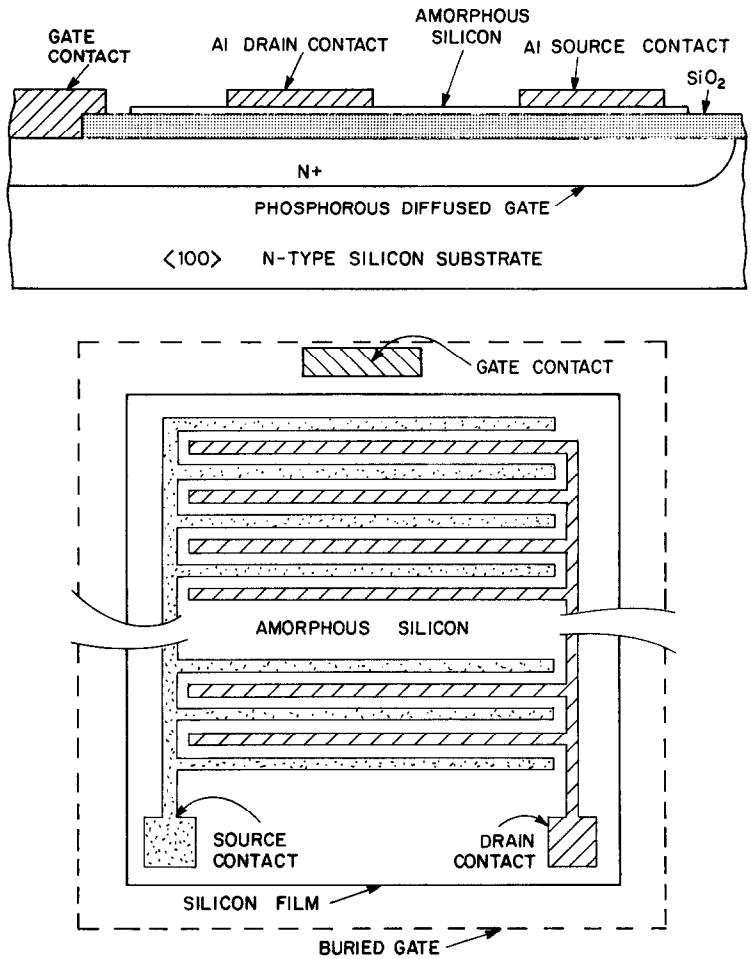

Fig. 1. Cross section and top view of a completed amorphous silicon TFT.

The substrate is first oxidized at 1200°C with zero grade dry oxygen flowing and a 3000 Å layer of SiO_2 is produced on the surface. This oxide is photolithographically etched with windows of 105 mil by 105 mil. Phosphorus is deposited for 20 min at 1000°C to form a 0.5 μ deep N^+ buried gate. The remaining oxide was completely stripped from the surface and a new high quality-low leakage oxide was thermally grown. This layer of SiO_2 serves as the insulator for the TFT.

The silicon–silicon dioxide substrate was then placed in a vacuum system equipped with an optically opaque liquid-nitrogen cryo-baffle. When the vacuum system reached its base pressure, the surface of the substrate was thermally etched by heating it to 300°C for one hour and then allowed to cool back towards room temperature. The amorphous silicon was electron beam evaporated immediately following the thermal etching and cooling. This step eliminated any hysteresis effects [7].

The deposition rate of the amorphous silicon was controlled using a water cooled quartz crystal deposition monitor. Amorphous silicon films nominally 500 to 700 Å thick were deposited at rates from about 3 to 5 Å/sec. Immediately after deposition the substrate was heated to 400°C and the amorphous film annealed for four hours without breaking vacuum. This anneal temperature is well below the crystallization temperature for the amorphous silicon [8]. Similar but much thicker films were determined to be amorphous under these fabrication conditions by X-ray diffraction and by heating the 700 Å film until an abrupt change in the conductivity was observed.

Five nines pure aluminium was evaporated over the entire structure and then selectively photolithographically etched to form the source, drain, and gate contacts as shown in the top view of Fig. 1. There were 40 interdigited fingers of 65 mil in length with 1 mil width and 1 mil spacing. Since the Si film was only about 600 Å thick and its resisitivity [9] is high (10^7 Ω-cm), the interdigited source-drain contact structure was used to increase the width to length ratio of the channel and allow a significant drain current to flow at zero gate voltage. The completed structures were tested for insulator leakage and instability before measuring the drain characteristics.

RESULTS

Figure 2 illustrates the drain current (I_D) vs drain voltage (V_D) for various values of gate voltage (V_G). This data is obtained for a TFT made from a 560 Å thick amorphous silicon film deposited at 3.2 Å/sec onto the 3000 Å thick SiO_2 substrate followed by a 400°C anneal for 4 hr. Note that the drain characteristics I_D vs V_D for a fixed value of V_G appear quite similar to an ordinary MOSFET. As the drain voltage, V_D, is increased

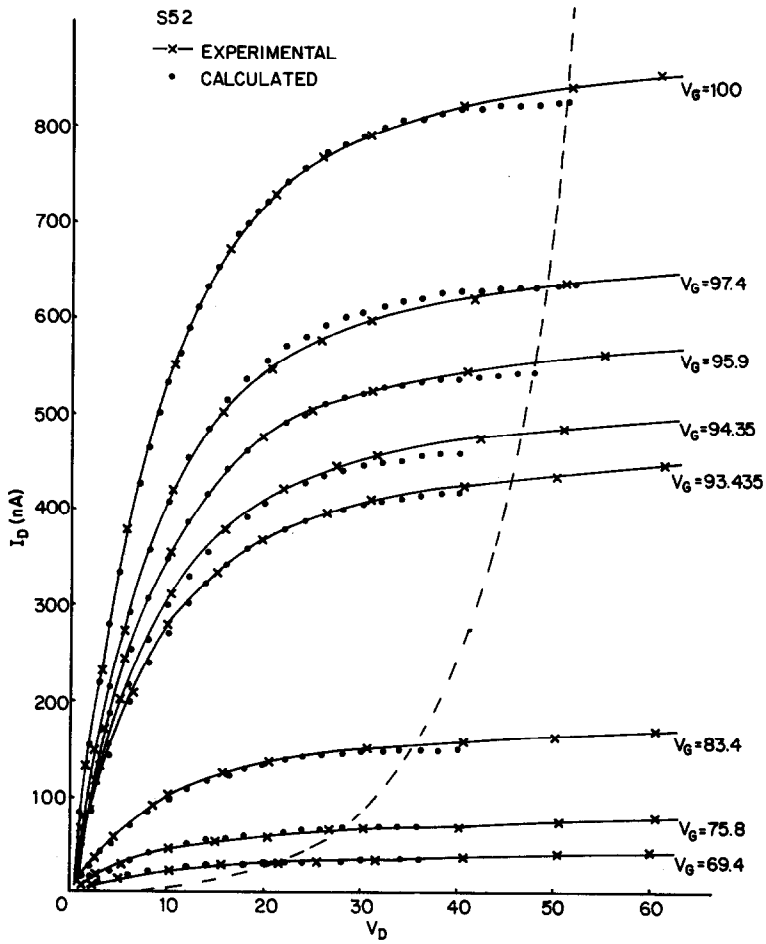

Fig. 2. Experimental and calculated drain characteristics for sample S52.

I_D increases but begins to saturate at larger values of V_D, indicating a channel pinch-off type condition. At these larger values of V_G and V_D there appears to be a channel shortening phenomenon or a leakage component present giving the beyond pinch-off region a slight slope to the straight line part of the plot.

The other important relationship for a field effect structure, the experimental V_G vs I_D at a very small value of V_D, ideally near zero, is shown in Fig. 3. This plot is for both positive and negative values of gate voltage, showing that the channel conductance can be modulated with either extended state, high mobility electrons or holes. Since the mobility for holes is less than that for electrons, this paper will concentrate mainly on positive gate voltages, or conduction via extended state electrons. The theoretical analysis and interpretation of Fig. 3 in terms of the density of localized states near the Fermi level is discussed in detail in Ref. [6].

SIMPLE THEORY

The development of the theory for an amorphous silicon TFT can be made along two lines. One is a very simple derivation based on the gate voltage channel conductance relationship of Fig. 3 and the other a more formal derivation. We shall first develop the simple theory and then show that an approximation to the formal theory leads to the same results, both of which are confirmed by experiment.

Tickle[1] shows that when only interior conduction occurs in the channel and when the gradual channel approximation is valid, the drain characteristics can be calculated using eqn (1).

$$I_D = \frac{W}{l}\int_{V_G-V_D}^{V_G} g(W)\,dW. \tag{1}$$

The function $g(W)$ is the sheet conductivity of the channel as a function of W, the potential difference between the gate and any point in the channel. Inspection of Fig. 3, for gate voltages of greater than about 50 V to less than 100 V, shows that the plot is nearly a straight line on the semi-log plot. This implies that an exponential relationship would describe the $g(W)$ function, since V_D is small compared to the gate voltage and is kept constant. Therefore, the potential difference becomes approximately equal to V_G in this range of voltages. By inspection of Fig. 3, the desired relationship can be written as eqn (2), where "a" is a function of the slope of the straight line portion of the plot and "b" is an arbitrary constant that will depend upon the carrier mobility, temperature, and geometrical factors of the device.

$$g(W) \doteq b\,e^{aW}. \tag{2}$$

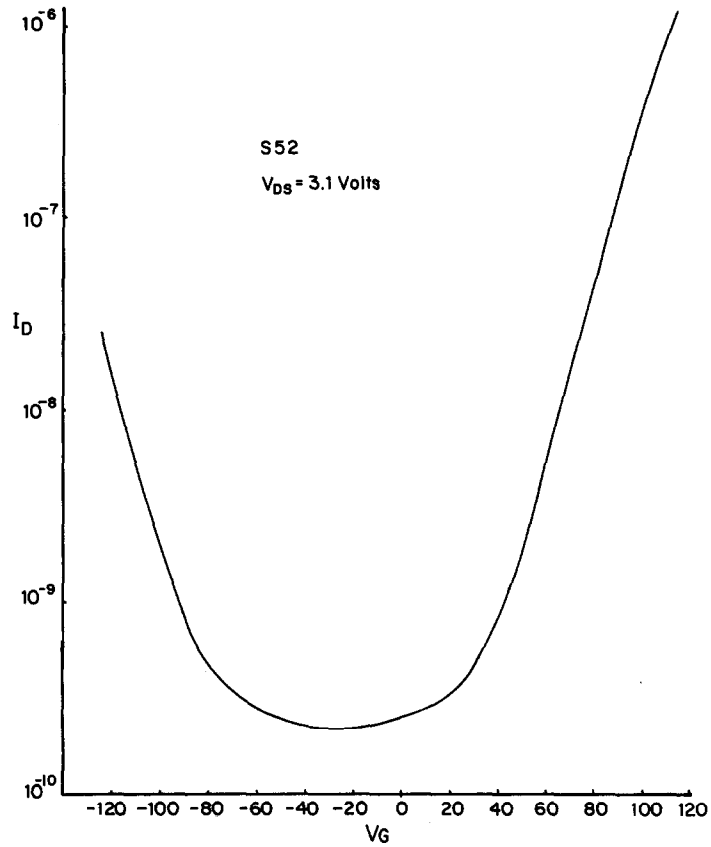

Fig. 3. The experimental plot of I_D vs V_G for a small fixed value of V_D for both positive and negative gate voltages.

Substituting the approximate relationship of eqn (2) into eqn (1) yields:

$$I_D \doteq \frac{wb}{l}\int_{V_G-V_D}^{V_G} e^{aW}\,dW$$

$$I_D \doteq \frac{wb}{la}[e^{aV_G} - e^{a(V_G-V_D)}] = B\,e^{aV_G}[1-e^{-aV_D}] \quad (3)$$

where B is a constant dependent upon the device parameters.

The functional relationship of eqn (3) for the drain characteristics of the device show that for a fixed V_G that I_D will saturate at large values of V_D. It should also be noted that eqns (1) and (3) only apply to the condition when the channel near the drain has not become pinched-off. The constant "a" in eqn (3) can be obtained from the slope of Fig. 3 for $50 \le V_G \le 100$ V. It can also be obtained from Fig. 2 for a fixed value of V_D since as indicated by eqn (3), if V_D is fixed then I_D is an exponential function of V_G. Figure 4 illustrates this case for two fixed values of V_D. The plots are identical except for a small leakage current component at the larger of the two drain voltages. For device S52 the value of "a" obtained from the slope of Fig. 3 is 0.102 with an uncertainty of ±0.002 while at least squares fit to the experimental points of Fig. 4 at V_D of 20 V yields a value of 0.1018. Also plotted in Fig. 4 is a comparison of the relationship as calculated from eqn (3) and the experimental points taken from Fig. 2, at a fixed value of V_D equal to 20 V. This plot shows the exponential relationship indicated by eqn (3) with a fixed value of V_D.

Figure 2 shows a plot of the family of calculated output characteristics for sample S52 using eqn (3), where the arbitrary constant "B" was obtained from

$$I_D = 31.2\times10^{-12}\,e^{0.1018V_G}[1-e^{-0.1018V_D}] \quad (4)$$

one point on either Fig. 2 or 4. The plots were calculated from eqn (4). This derivation is based on below pinch-off operation and that the exponential relationship is valid. Hence, for gate voltages less than 50 V eqn (4) becomes invalid as is indicated by the dashed line of Fig. 2. Figure 5 illustrates a similar plot of the experimental and calculated data for gate voltages to as low as 54.6 V and with an expanded scale near the origin. Each device tested was modeled with similar accuracy. Other examples are shown in Fig. 6 and 7 for devices with different densities of localized states in the bandgap produced by changing the rate of evaporation of the amorphous silicon.

THEORY

Most of the basic theory for the TFT is based upon the theoretical explanation and experimental verification of the $g(W)$ plot similar to Fig. 3. These calculations have been presented by the authors in detail in Ref. [6] and will be only briefly described here. The analysis assumes that the density of localized states model for amorphous silicon is that proposed by Cohen-Fritzsche-

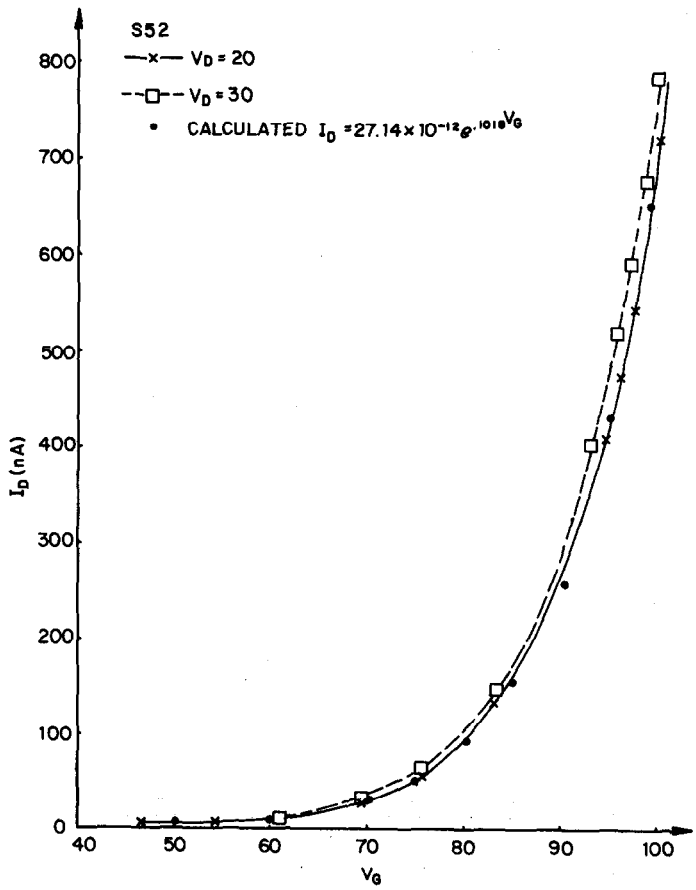

Fig. 4. The drain current vs gate voltage for fixed values of V_D.

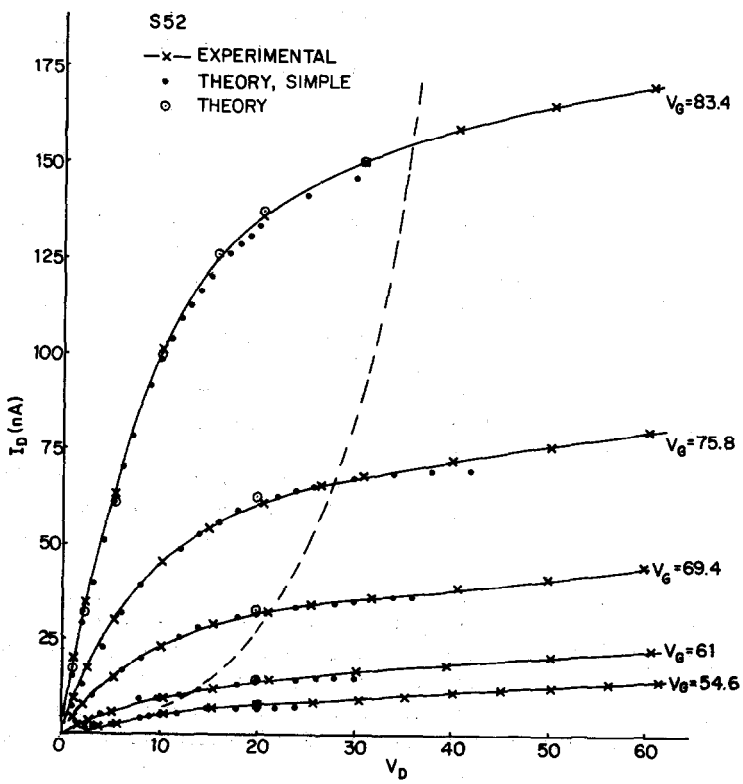

Fig. 5. The drain characteristics for sample S52.

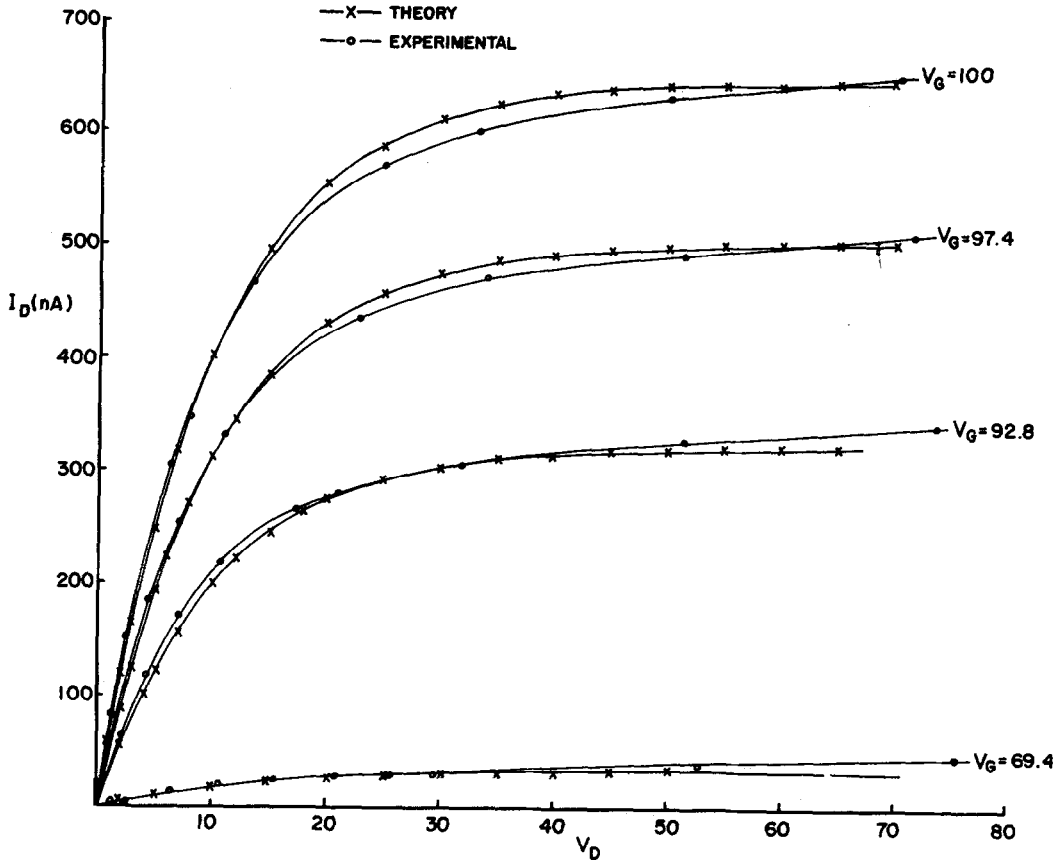

Fig. 6. The drain characteristics for a TFT device with a different density of localized states.

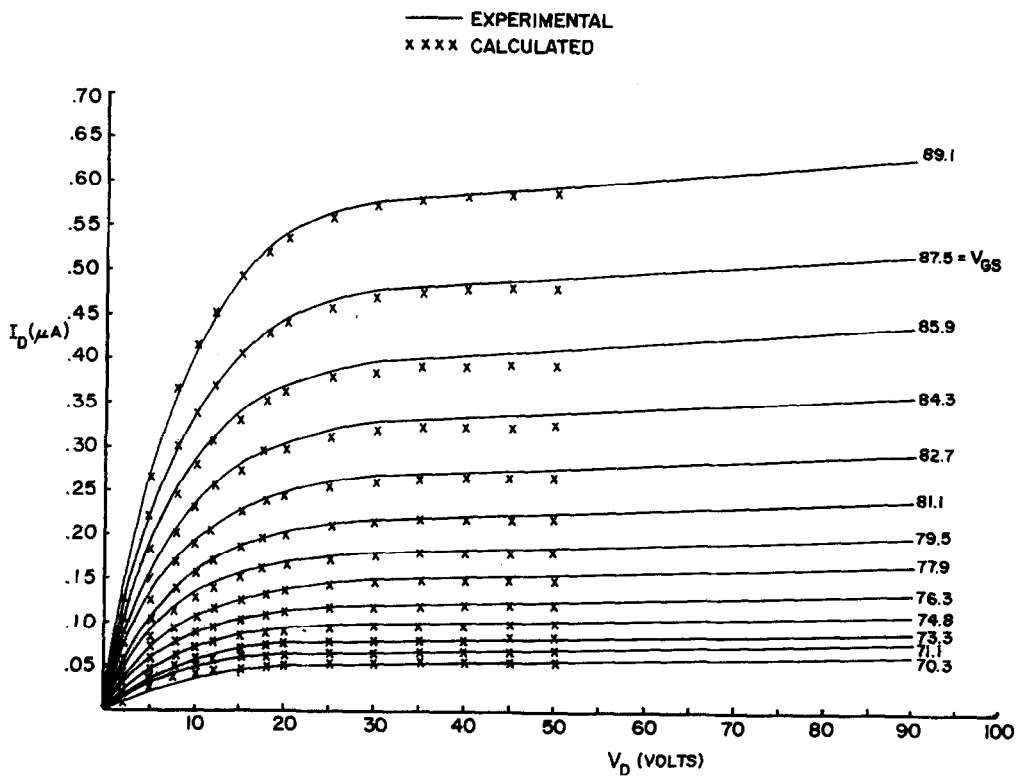

Fig. 7. An amorphous silicon TFT with different parameters than those of Figs. 5 and 6.

Ovshinky[9]. This model for the density of electronic states provides for extended state conduction, which is similar to the valence band and conduction band of crystalline semiconductors, and for tailing of these bands due to the lack of long range order in the material. Nearest neighbor tetrahedral bonding is preserved and to some extent next nearest neighbor, with most of the disorder coming in the form of bond angle deviations. In their model these tails of localized states may have significant overlap. By assuming that these localized states, N_T, overlap in such a way that they are in effect uniform throughout the bandgap, it has been shown[7] that the plots of I_D vs V_G, at a small fixed value of V_D, can be calculated for positive as well as negative gate voltages and at various temperatures. The calculated and experimental plots agree well over a range of positive and negative gate voltages, as well as temperatures.

The derivation begins with the definition of the energy band bending parameter $\xi(X)$ which measures the amount the electron energy bands have bent from their fixed bulk level as the amorphous silicon–silicon dioxide interface is approached.

The x-axis is chosen at this interface and x increases into the amorphous silicon. For positive gate voltages the electron energy band is bent downward at the surface and $\xi(X)$ is taken as a positive quantity.

Applying Poisson's equation for the case of N_T being independent of energy, i.e. a uniform distribution of states, yields eqn (5).

$$\frac{d^2\xi(X)}{dx^2} = \frac{q^2}{\epsilon} N_T \xi(X). \tag{5}$$

This equation is easily solved for $\xi(X)$ and shows the band bending to be exponential.

$$\xi(X) = \xi(0)\exp(-Lx). \tag{6}$$

The value of L is given by eqn (7) where a larger density of states

$$L = \left(\frac{q^2 N_T}{\epsilon}\right)^{1/2} \tag{7}$$

leads to a smaller active channel thickness for a given $\xi(0)$, the value of the band bending at the surface.

Typical values of N_T might be as large as $10^{20}/\text{cm}^3$ eV yielding a $1/L$ of 25.8 Å. Therefore only a small part of the 600 Å amorphous silicon film has significant band bending and hence conductance modulation. The silicon dioxide thickness is 3000 Å; therefore, the semiconductor capacitance is much larger than the silicon dioxide capacitance. Since these capacitors are in series we can use arguments similar to that for a MOS structure to show that the potential difference, W, between the gate and any point in the channel can be written in terms of the band bending parameter at the surface, $\xi_s = \xi(0)$.

$$W \doteq \frac{\epsilon d}{\epsilon_{ox} q} L\xi_s. \tag{8}$$

The silicon dioxide thickness is d and the dielectric constant ϵ_{ox}. Since the potential difference W will vary along the channel, so will ξ_s and vice versa.

The sheet conductance of the total high conductance channel is

$$G_s = q\mu_n \int_0^t n\,dx + q\mu_p \int_0^t p\,dx \tag{9}$$

and with no gate voltage applied is given by eqn (10) where t is the thickness of the amorphous silicon film.

$$G_{s0} = qt(\mu_n n_b + \mu_p p_b). \tag{10}$$

From Fig. 3 it may be seen that the change in sheet conductance, $\Delta G_s = G_s - G_{s0}$, in the region of interest is over 3 orders of magnitude. By assuming the extended state conduction of obey Maxwell–Boltzman statistics we can write

$$\Delta G_s = \frac{q\mu_n n_b}{L}\int_0^{\xi_s} \frac{\exp[\xi/kT]-1}{\xi}\,d\xi + \frac{q\mu_p p_b}{L}\int_0^{\xi_s} \frac{\exp[-\xi/kT]-1}{\xi}\,d\xi. \tag{11}$$

From eqn (8) the band bending parameter at the surface can be written in terms of the potential as

$$\xi_s = \frac{qW\epsilon_{ox}}{d\,L\epsilon}. \tag{12}$$

Equation (11) then becomes the basic relationship of $g(W) = \Delta G_s$ needed for the calculation of the drain current using eqn (1). Substituting eqn (11) into eqn (1) yields eqn (13).

$$I_D = \frac{w}{l}\int_{V_G - V_D}^{V_G} \left[\frac{q\mu_n n_b}{L}\int_0^{\xi_s(W)} \frac{\exp[+\xi/kT]-1}{\xi}\,d\xi + \frac{q\mu_p p_b}{L}\int_0^{\xi_s(W)} \frac{\exp[-\xi/kT]-1}{\xi}\,d\xi\right] dW. \tag{13}$$

With a large positive gate voltage the second term of the above equation becomes negligible, especially when there is a significant amount of band bending to create a large conductance modulation. Equation (13) can then be approximated as

$$I_D \doteq \frac{w}{l}\int_{V_G - V_D}^{V_G} \left[\frac{q\mu_n n_b}{L}\int_0^{\xi_s(W)} \frac{\exp[\xi/kT]-1}{\xi}\,d\xi\right] dW. \tag{14}$$

The inner integral cannot be easily evaluated without the aid of a digital computer and numerical integration techniques. However, it can be approximated by a power series and then integrated as follows:

$$\int_0^{\xi_s/kT} \frac{\exp(\xi/kT)-1}{\xi/kT}\,d\left(\frac{\xi}{kT}\right) \doteq \sum_{n=1}^{\infty} \frac{(\xi_s/kT)^n}{nn!} = S. \tag{15}$$

With the aid of eqn (12) and the definition of η

$$\frac{\xi_s}{kT} = \frac{q\epsilon_{ox}}{d\,L\epsilon kT} W = \eta W \tag{16}$$

the sheet conductance change can be written as eqn (17)

$$g(W) = \frac{q\mu_n n_b}{L} \sum_{n=1}^{\infty} \frac{(\eta W)^n}{nn!}. \tag{17}$$

Now eqn (17) can be substituted into eqn (1) and integrated.

$$I_D = \frac{w}{l} \frac{q\mu_n n_b}{L} \int_{V_G - V_D}^{V_G} \sum_{n=1}^{\infty} \frac{(\eta W)^n}{nn!} dW. \tag{18}$$

Therefore the drain characteristics can be written in terms of the infinite series.

$$I_D = \frac{wq\mu_n n_b}{lL} \left\{ \sum_{n=1}^{\infty} \frac{\eta^n V_G^{n+1}}{n(n+1)(n!)} - \sum_{k=1}^{\infty} \frac{\eta^k (V_G - V_D)^{k+1}}{k(k+1)k!} \right\}. \tag{19}$$

To verify eqns (17) or (19) it is necessary to know the product $\mu_n n_b$, not an easy task for amorphous materials. One could assume μ_n to be nearly that of single crystalline silicon and then attempt to determine n_b from an independent experiment for the conductivity. However, as in most FET analyses μ_n is not the bulk mobility and must be an assumed value and is dependent upon the normal and longitudinal field. Since the semiconductor material is amorphous and shows no long range order the subject of the surface and the mobility dependence with electric field is open for consideration. Here we select μn_b as a constant necessary to fit the experimental data at one point.

For sample S52 illustrated in Figs 2–5 $N_T = 9 \times 10^{19}$ (from Ref. [6]), $d = 3000$ Å, $1/L = 27.157$ Å, $\epsilon_{ox} \doteq 4\epsilon_0$, and $\epsilon \doteq 12\epsilon_0$. Then η calculates to be equal to 0.1167 for this device. A plot of eqn (15) is illustrated in Fig. 8 for S52 over the range of gate voltages of interest. Note that it plots as a straight line on the semi-log plot between gate voltages of 50–100 V. Also plotted is the straight line portion of Fig. 3, the experimental data, for sample S52 to show that the simple assumption of $g(W)$ to be an exponential relationship is quite good. When the "a" term of eqn (3) is obtained from the s-plot of Fig. 8, $a = 0.100 \pm 0.002$ as compared to 0.102 ± 0.002 from the experimental data. Both of these agree very well with the value $a = 0.1018$ used in eqn (4) and plotted in Figs. 2 and 5.

Equation (19) can be calculated using the same parameters, and the results are in excellent agreement with the experimental data. Figure 5 illustrates several of the calculated and experimental points for $V_G = 83.4$ V over a range of V_D. Note the general agreement between the theory and the experiment. Also plotted in Fig. 5 are calculated values of I_D for V_D fixed at 20 V for a range of gate voltages from 54.6 to 83.4 V. This shows that eqn (19) can be used to accurately calculate the entire set of I_D characteristics using one selected value of $\mu_n n_b$.

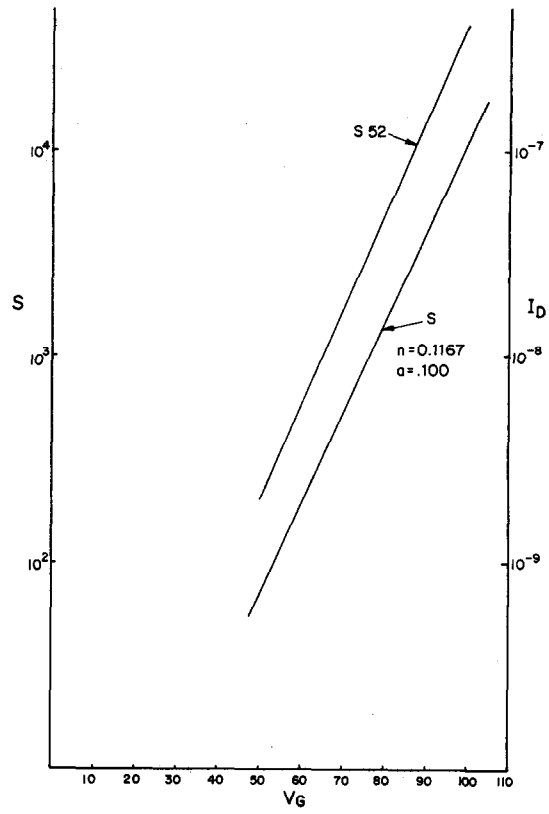

Fig. 8. The S-plot of eqn (11) for sample S52 and the straight line portion of Fig. 3.

CONCLUSIONS

The drain characteristics for a thin film transistor with a uniform distribution of localized states in the band gap have been calculated and verified experimentally. An amorphous silicon TFT was shown to be possible using a buried N^+ region for a gate and silicon dioxide as the insulator. The amorphous silicon was electron beam evaporated and the rate carefully controlled so that the density of localized states can be kept small enough to observe any significant conductance modulation.

The simple theory, obtained by assuming an exponential relationship between V_G and the channel conductance, fits the experimental data surprisingly well. The data fits over a large range of V_G and V_D out to the "pinch-off" of the channel. A more complete derivation shows that the exponential assumption is justified in the range of V_G considered since the infinite series solution plots as a straight line of the semi-log scales. In addition the "a" obtained by the experimental data agrees very well with the calculated value. Calculating the drain characteristics directly from the infinite series solution leads to little, if any, improvement over the simple solution; both of which agree well with the experimental data.

It should be stated that the TFT's reported here have in no way been optimized in geometry or for larger conductance changes that could be obtained from a thinner oxide or from hydrogen incorporation into the amorphous silicon during fabrication [10].

REFERENCES

1. A. C. Tickle, *Thin Film Transistors*. Wiley, New York (1969).
2. P. K. Weimer, *Proc. IRE* 50, 1462 (1962).

3. A. van Calster and H. J. Pauwels, *Solid-St. Electron.* **18**, 691 (1975).
4. T. A. DeMassa and H. I. Refioglu, *Solid-St. Electron.* **18**, 315 (1975).
5. A. K. Malhotra and G. W. Neudeck, *Appl. Phys. Lett.* **24**, 29 (1974).
6. G. W. Neudeck and A. K. Malhotra, *J. Appl. Phys.* **46**, 2662 (1975).
7. G. W. Neudeck and A. K. Malhotra, *J. Appl. Phys.* **46**, 239 (1975).
8. N. A. Blum and C. Feldman, *J. Non-Cryst. Solids* **11**, 242 (1972).
9. M. H. Cohen, H. Fritzsche and S. R. Ovshinsky, *Phys. Rev. Lett.* **22**, 1065 (1969).
10. A. K. Malhotra and G. W. Neudeck, *Appl. Phys. Lett.* **28**, 47 (1976).